TRANSMITTAL FORM

Attorney Docket No. RPS920010127US1/2280P

In re the application: Robert T. BAILIS et al.

Confirmation No: 5286

Serial No: 10/016,449

Group Art Unit: 2133

Filed: December 10, 2001

Examiner: Tabone Jr., John J.



For: Method and System for Use of a Field Programmable Gate Array (FPGA) Function within an Application Specific Integrated Circuit (ASIC) to Enable Creati

		•		ENCL	OSURES (check all	that apply))	_		
•	Amendment/Reply				Assignment and Recordation Cover Sheet			After Allowance Communication to Group		
	After Final				Part B-Issue Fee Transmittal			Notice of Appeal		
	Information disclosure statement				Letter to Draftsman			Appeal Brief (in triplicate)		
	Form 1449			Drawings			Status Letter			
		(X) Copies	s of References	es Petition				Postcard		
	Extension of Time Request *			Fee Address Indication Form			Other Enclosure RECEIVED identify below):		Þ	
	Express Abandonment				Terminal Disclaimer		SEP 2 0 200			
	Certified Copy of Priority Doc				Power of Attorney and Revocation of Prior Powers		Technology Center 210			10
	Response to Incomplete Appln				Change of Correspondence Address					
	Response to Missing Parts *Extension of Term: Pursuant to 37 CFR 1.136, Applicant petitions the Commissioner to extend the time for response for two month(s), from July 13, 2004 to September 14, 2004.									
]	<u> </u>		_l	CLAIMS				-	1
	FOR Claims Remain After Amendme				Highest # of Claims Previously Paid For	Extra Cla	aims	RATE	FEE	
Total	Claim	s	15		20	0		\$18.00	\$ 0.00	1
Indep	ndependent Claims		2		3	0		\$86.00	\$ 0.00	1
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	Check no. 8039 in the amount of \$420.00 is enclosed for payment of extension fees.									
	Charge \$ to Deposit Account No (Account Holder Name) for payment of fees.									
	Charge any additional fees or credit any overpayment to Deposit Account No. 50-0563 (IBM Corporation).									
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Signa	ature		June	u] Š
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 13, 2004.

Jinny Ngayen (

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Date: September 13, 2004

Robert T. BAILIS et al.

Confirmation No. 5286

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Examiner: Tabone, Jr., John J.

For:

METHOD AND SYSTEM FOR USE OF A FIELD PROGRAMMABLE GATE

ARRAY (FPGA) FUNCTION WITHIN AN APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) TO ENABLE CREATION OF A

DEBUGGER CLIENT WITHIN THE ASIC

Mail Stop Amendment Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

RECEIVED

SEP 2 0 2004

AMENDMENT

Technology Center 2100

Sir:

In response to the Office Action dated April 14, 2004, Applicant submits the following amendments and remarks:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 6 of this paper.